DATA SHEET

74F579
8-bit bidirectional binary counter (3-State)

Product specification
Supersedes data of 1992 May 04

2000 Dec 18

Philips
Semiconductors

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8-bit bidirectional binary counter (3-State) 74F579

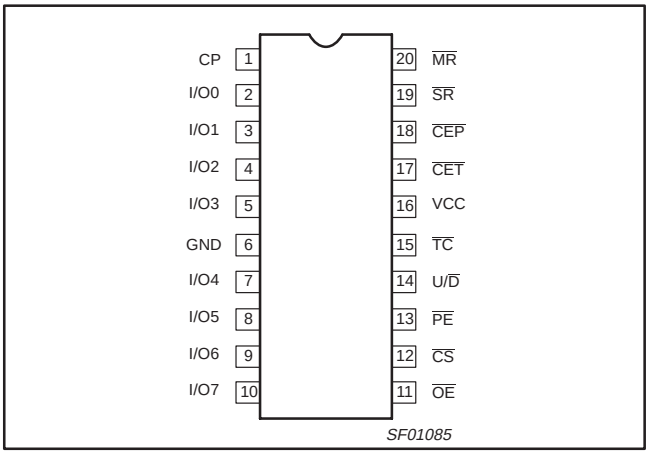
FEATURES

- Fully synchronous operation
- Multiplexed 3-State I/O ports for bus oriented applications
- Built in cascading carry capability
- U/$\overline{D}$ pin to control direction of counting
- Separate pins for Master reset and Synchronous operation
- Center power pins to reduce effects of package inductance
- Count frequency 115 MHz Typ
- Supply current 100 mA Typ
- See 74F269 for 24-pin separate I/O port version
- See 74F779 for 16-pin version

DESCRIPTION

The 74F579 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-State I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock. $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

PIN CONFIGURATION



ORDERING INFORMATION

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F579	115MHz	100 mA

ORDERING INFORMATION

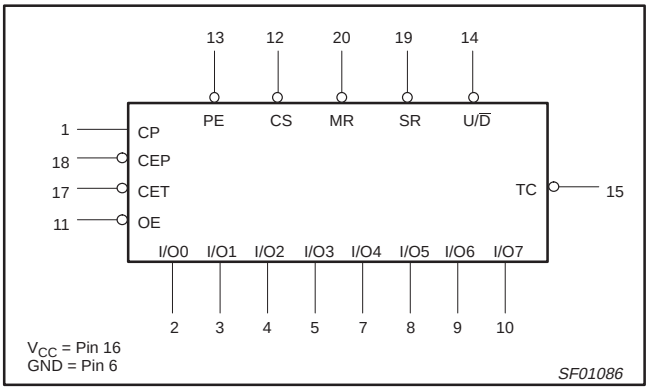
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5 V ±10%, T_{amb} = 0 to +70 °C	PKG DWG #
20-Pin Plastic DIP	N74F579N	SOT146-1
20-Pin Plastic SOL	N74F579D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

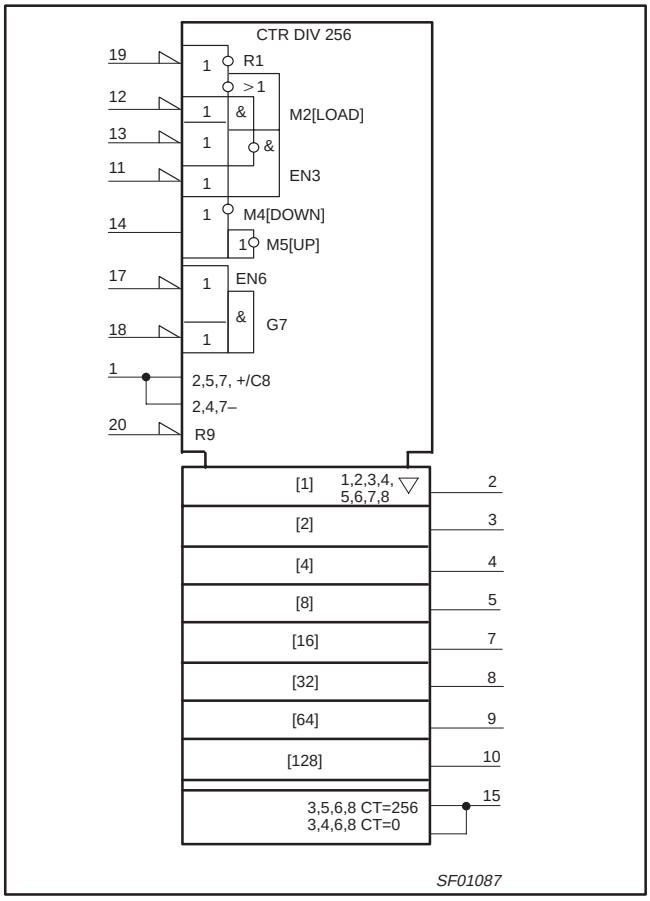
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH / LOW
I/O_n	Data Inputs	3.5/1.0	70 µA / 0.6 mA
	Data Outputs	150/40	3.0 mA / 24 mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20 µA/ 0.6 mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20 µA / 0.6 mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20 µA / 0.6 mA
$\overline{SR}$	Synchronous Reset input (active Low)	1.0/1.0	20 µA / 0.6 mA
$\overline{CEP}$	Count Enable Parallel input (active Low)	1.0/1.0	20 µA / 0.6 mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20 µA / 0.6 mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20 µA / 0.6 mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20 µA / 0.6 mA
CP	Clock input (active Rising Edge)	1.0/1.0	20 µA/ 0.6 mA
$\overline{TC}$	Terminal Count Output (active Low)	50/33	1.0 mA / 20 mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 µA in the High state and 0.6 mA in the Low state.

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

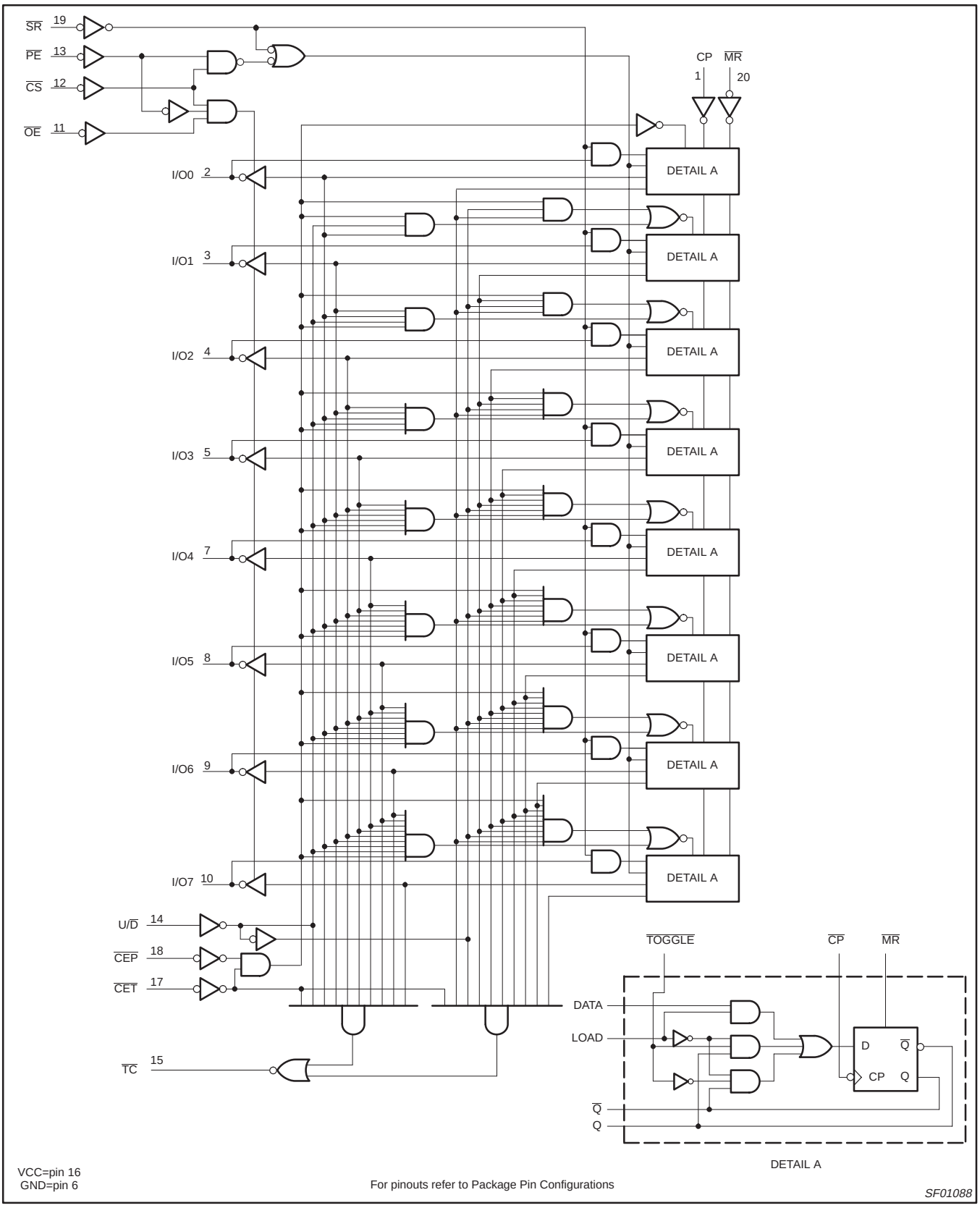


FUNCTION TABLE

INPUTS									OPERATING MODE
$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	$\overline{OE}$	$\overline{CP}$	
X	X	H	X	X	X	X	X	X	I/O0 to I/O7 in high impedance ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/O0 to I/O7 in high impedance
X	X	L	H	X	X	X	L	X	Flip-flop output appears on I/On lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held High)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = $\overline{CS}$ and $\overline{PE}$ should never be Low voltage level at the same time.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_O	Voltage applied to output in High output state		–0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/O0	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	$\overline{TC}$			–1	mA
		I/O_n			–3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/O_n			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN (V_{IL} = 0.0 V, V_{IH} = 4.5 V for $\overline{MR}$, CP inputs)	I_{OH} = –1 mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH} = –3 mA	±10%V_{CC}	2.4	3.3		V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX,	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} = MAX, V_I = 5.5 V					1	mA
		others	V_{CC} = MAX, V_I = 7.0 V					100	µA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7 V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5 V					–0.6	mA
I_{OZH}+ I_{IH}	Off-state output current High-level voltage applied	I/O_n	V_{CC} = MAX, V_O = 2.7 V					70	µA
I_{OZL}+ I_{IL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5 V					–600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				95	135	mA
		I_{CCL}					105	145	mA
		I_{CCZ}					105	150	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions for the applicable type.
2. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

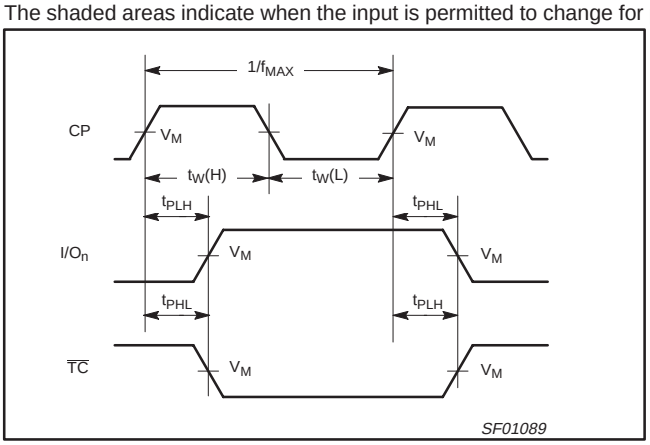
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0 to +70 °C V_{CC} = +5.0 V ± 10% C_L = 50 pF, R_L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	5.0 5.0	7.5 7.5	10.5 10.5	4.5 5.0	11.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 5.5	7.5 7.5	10.0 10.0	5.0 5.0	11.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 4	3.5 4.5	5.5 6.5	8.0 8.0	3.5 4.5	9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 3	3.5 3.5	5.5 6.0	7.0 8.0	3.5 3.5	8.5 8.5	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	7.0	9.0	5.0	10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{TC}$	Waveform 4	4.0 6.0	6.5 8.0	9.0 10.5	4.0 6.0	10.5 12.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{CS}$ to I/O_n	Waveform 6 Waveform 7	4.0 5.5	5.0 7.0	8.5 10.5	3.5 5.0	10.0 11.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{CS}$ to I/O_n	Waveform 6 Waveform 7	3.0 5.0	5.0 7.5	7.5 9.5	3.0 4.5	9.0 11.0	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	3.0 5.0	4.5 6.5	8.0 10.0	3.0 4.5	9.0 11.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	3.0 2.5	4.0 4.0	7.5 7.5	3.0 2.0	9.0 8.5	ns ns
t_{PZH} t_{PZL}	Output Disable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	2.5 4.5	4.0 5.5	7.0 9.0	2.5 4.0	8.5 10.5	ns ns
t_{PHZ} t_{PLZ}	Output Enable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	1.0 2.0	2.5 4.0	4.0 7.0	1.0 2.0	5.5 8.0	ns ns

AC SETUP REQUIREMENTS

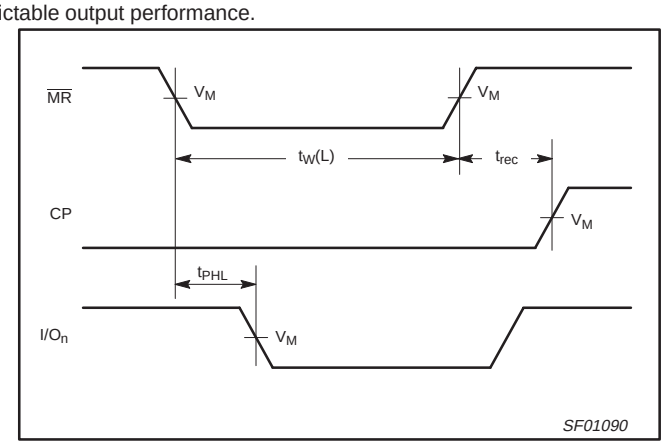
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0 to +70 °C V_{CC} = +5.0 V ± 10% C_L = 50 pF, R_L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 5	3.0 3.0			4.0 4.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 5	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	Waveform 5	8.0 8.0			9.0 9.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP	Waveform 5	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	9.5 9.5			10.0 10.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	5.0 9.0			5.5 10.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.5 4.5			4.5 4.5		ns ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	3.0			3.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

AC WAVEFORMS

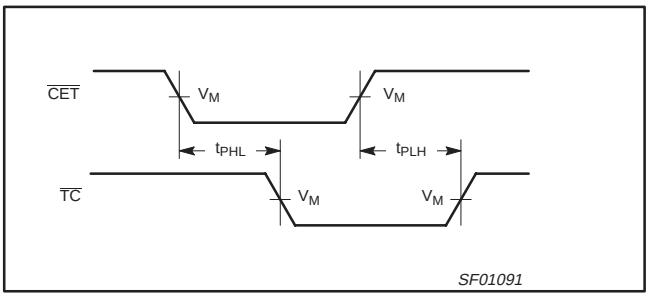
NOTE: For all waveforms V_M = 1.5 V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



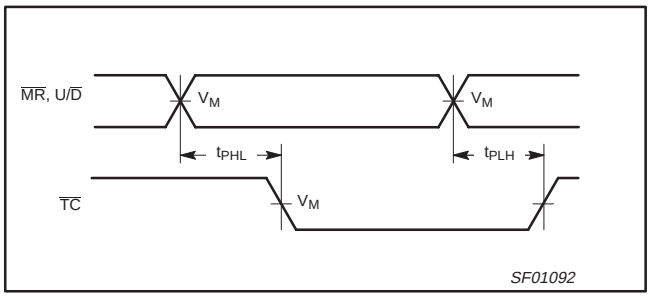
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



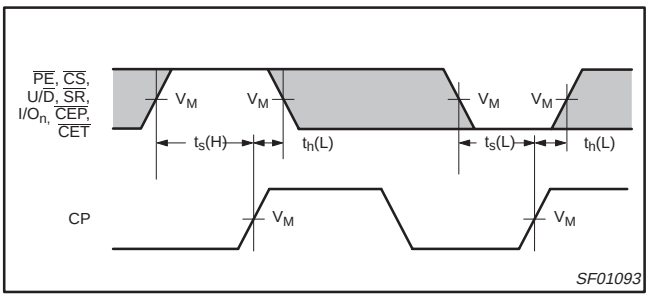
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



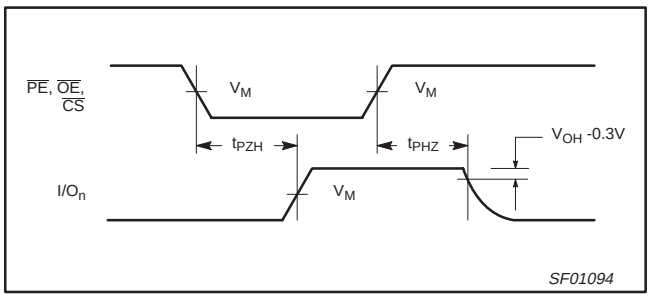
Waveform 3. Propagation Delay, $\overline{CET}$ Input to Terminal Count Output



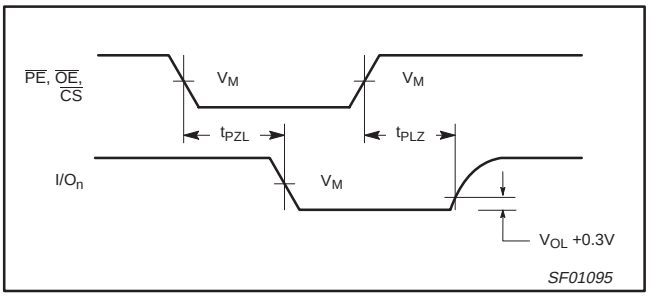
Waveform 4. Propagation Delay, U/$\overline{D}$ and $\overline{MR}$ Inputs to Terminal Count Output



Waveform 5. Setup and Hold Times

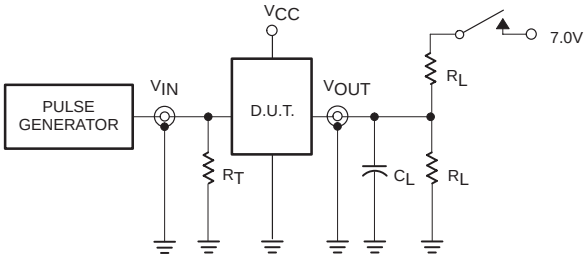


Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level

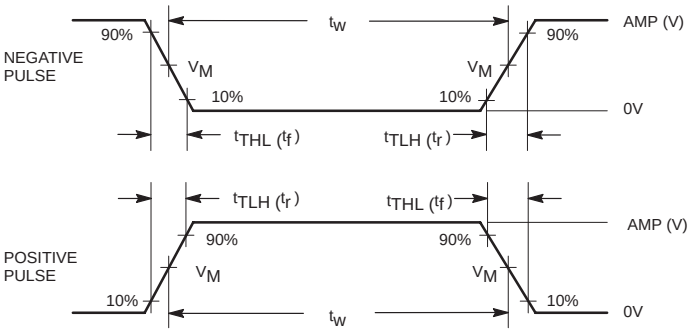


Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

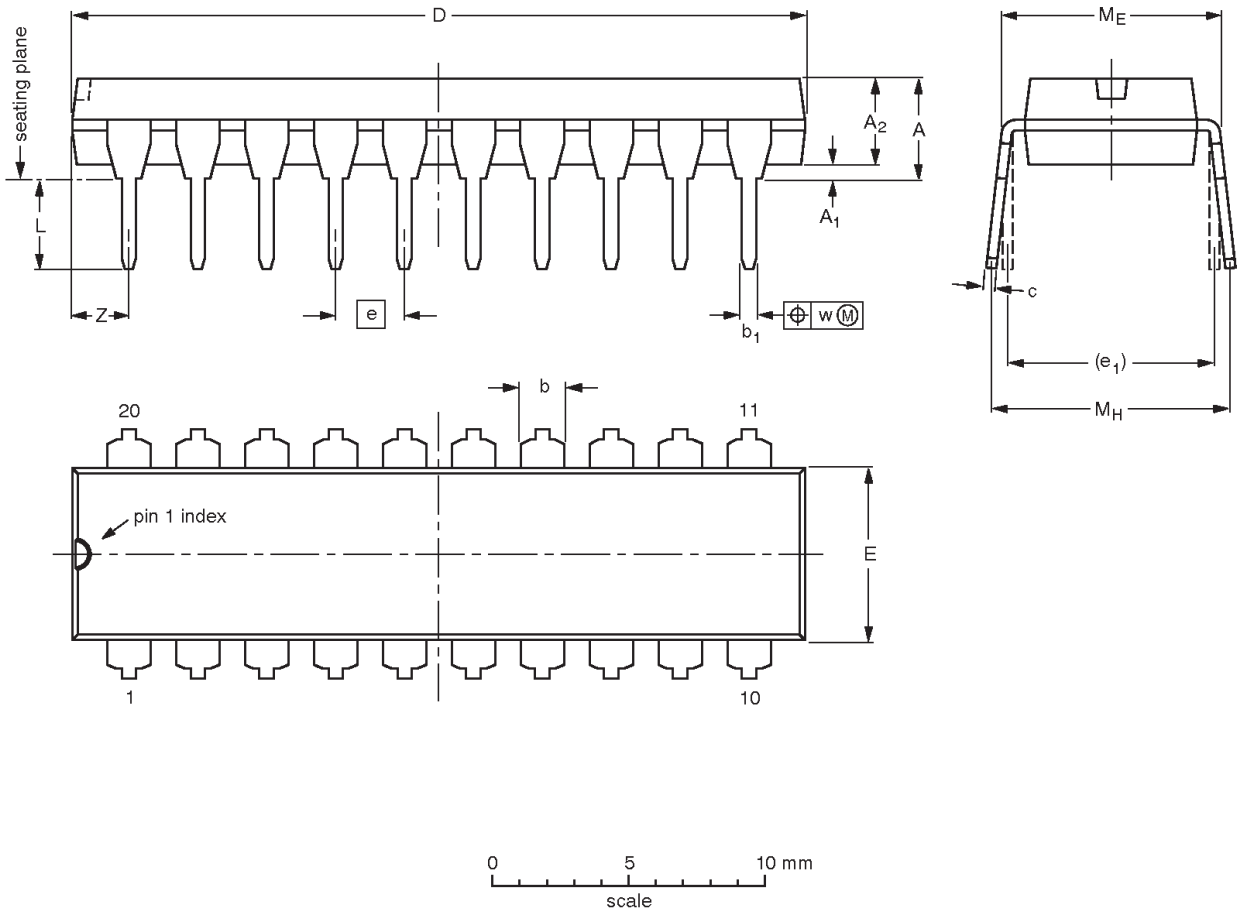
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

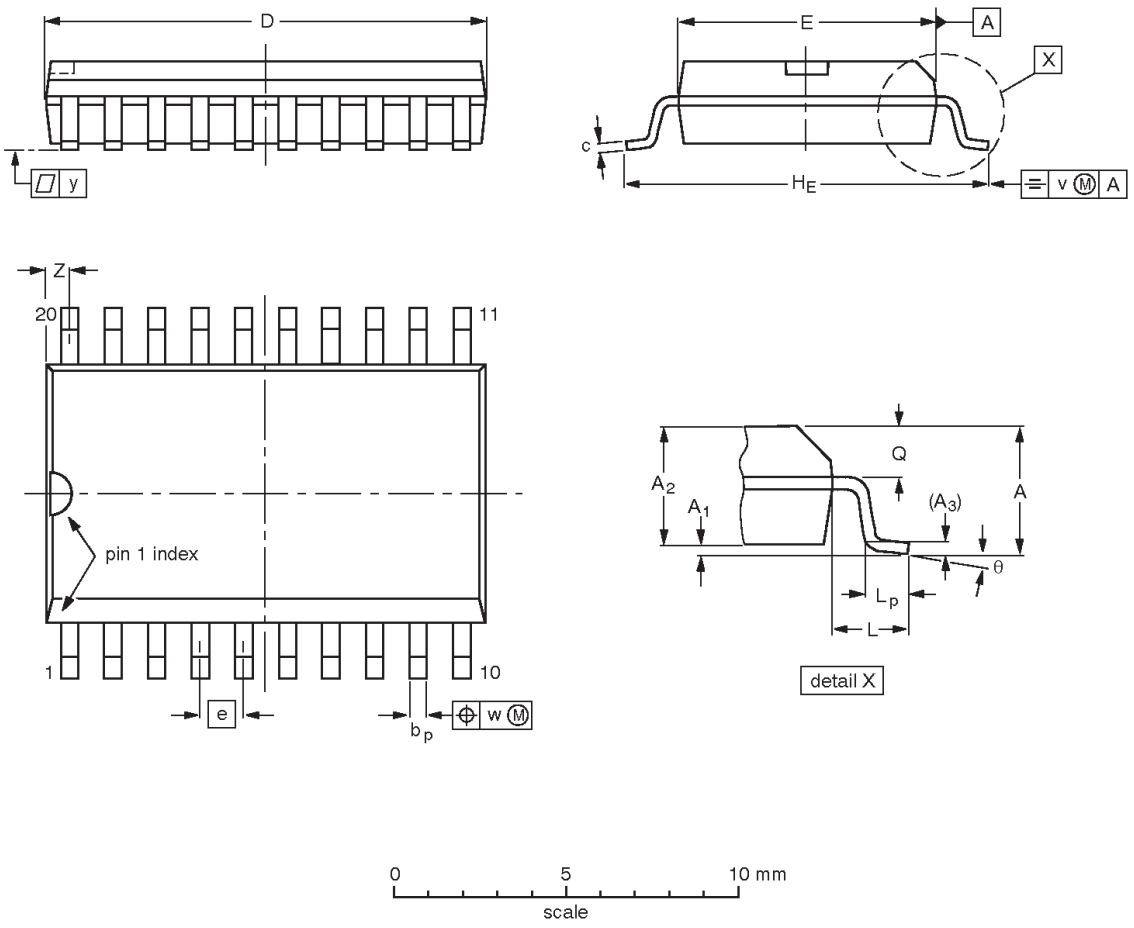
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1		MS-001	SC-603			~~95-05-24~~ 99-12-27

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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